Dock. 95-42

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April 26, 1990

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APR 26 1990

Federal Communications Commission
Office of the Secretary

Ms. Donna R. Searcy
Secretary
Federal Communications Commission
1919 M Street, N.W.
Washington, D.C. 20554

Re: A. C. Nielsen Company's Request for Use of Line 22 of the Active Portion of the TV Signal
File No.: DA 89-1060
Ex Parte Presentation

Dear Ms. Searcy:

This is to note that on April 26, 1990, Bruce H. Turnbull and Ronald W. Kleinman of Weil, Gotshal & Manges, on behalf of VidCode Inc., met with Roy Stewart, Chief of the Mass Media Bureau, Robert Ratcliffe, Assistant Chief of the Bureau, and William Hassinger, Assistant Chief (Engineering) to discuss the above-referenced matter.

The discussion related to the substance of the documents previously filed on behalf of VidCode in this matter. In addition, VidCode submitted for consideration by the Commission and discussed with the participants in the meeting the attached catalogue of Valley Stream Group, Ltd. We also pointed out observations by VidCode engineers of AMOL overwriting of commercial broadcasts occurring on April 25, 1990.

Should any question arise concerning this matter, please contact me.

Respectfully submitted,

Bruce H. Turnbull

Bruce H. Turnbull
Counsel for VidCode

cc: Mr. Roy J. Stewart
Mr. Robert H. Ratcliffe
Mr. William Hassinger
Grier C. Raclin, Esq.
David E. Hilliard, Esq.
John D. Pellegrin, Esq.

VALLEY STREAM GROUP, LTD.

[redacted]E
VALLEY STREAM, NEW YORK 11581
TELEPHONE 516-[redacted]
568 9449

VALLEY STREAM GROUP
28 FOURTH STREET
VALLEY STREAM, N.Y. 11581

SID - GENERATOR
READER
M-SGR-38

VALLEY STREAM GROUP, LTD.

28 FOURTH STREET
VALLEY STREAM, NY 11581
516-568-9449

*** PROGRAMMING NOTICE ***

In addition to programming the unit via the front panel switches, the MSGR-38 supports a serial protocol.

The command format to the MSGR-38 is: the two digit command header, followed by data (if required), followed by a carriage return.

i.e. I D M E D I A cr

The following commands have been added to the MSGR-38:

ID a b c d e - Program ID name - loads the data specified by abcde into the syndicator ID field (frames 20,21). The data may be ASCII characters in the range of 20H to 5AH.

TT a b c d e - Program Title - loads the data specified by abcde into the title field (frames 22,23). The data may be ASCII characters in the range of 20H to 5AH.

EP a b c d e - Program Episode - loads the data specified by abcde into the episode field (frames 24,25). The data may be ASCII characters in the range of 20H to 5AH.

Each of the above commands automatically stores the data in non-volatile EEPROM. There is no need to follow them with an XD command.

SID GENERATOR READER
SGR-38

Instruction Manual

Contents

SGR-38, Description

General:

The SGR-38 (SID Generator-Reader) was designed to read, generate and insert the Source IDentification code on field one, line twenty of a video signal.
In addition, the unit can control a satellite uplink exciter in response to a special vertical interval code.

- o microprocessor controlled:
  80C31 microcontroller with 8K of program memory, 74HCxyz series of logic combined with CMOS programmable logic arrays to reduce component count and power usage.

- o SID reader:
  complete SID reader function which can be used to synchronize the internal clock.

- o internal Real Time Clock:
  crystal controlled clock with battery back-up used to generate month,day,hour,minute,second, for the SID generator.

- o SID generator:
  complete SID generator with phase locked 64xH clock for stable position, and the ability to insert 30 ASCII characters into frames 4 thru 15 (5 per 2 frames), and 10 characters in frames 16 thru 19 (5 per 2 frames).

- o 2x1 SID delete/insert:
  the video circuits include a 2x1 switch to delete the old SID and insert new SID.

- o eight character alpha-numeric display:
  front panel LED display for operator assistance, status, and programming of information to be inserted.

- o black output:
  the SGR generates a B&W (no burst or setup) video signal with SID when input video is removed.

- o exciter control:
  the SGR reads the Exciter Control Code (ECC) on line 10 of the input video and controlls the satellite exciter in response to that code.

- o RS-232C port:
  a 300 baud asynchronous communications port permits data entry from a remote computer, terminal or modem.

INSTALLATION:

```
**************************************************************
*                        ! CAUTION !                         *
**************************************************************
* ! Do NOT operate the SGR-38 without a safety ground.  ! *
* ! A protective ground connection, via the power cord  ! *
* ! is essential for safe operation.                    ! *
**************************************************************
```

1. Connect the video source to the Program Video Input. Do NOT terminate, as the SGR38 contains its own internal 75 ohm termination. It is recommended that the Program Video Input be fed by one dedicated output of an equalizing DA, with a 75 ohm resistive source impedance.

2. Connect the video destination to the Program Video Output. Terminate with 75 ohms. Both the Program Video Output and the Monitor Video Output are 75 ohm resistive build-outs.

3. Connect the EXC CNTL output to the exciter control input, if required. Do NOT terminate this line; it is a TTL level signal.

4. Apply Power, 115VAC 60Hz 10VA.

5. The unit will display the current time of the internal real time clock, in the format HH:MM:SS. The clock has been preset to Network time, do not reset it to local time.

6. Verify that the SGR38 is generating a SID signal on line twenty, field one, source number =255 (see Operation, Display a Mode, SID OUT). ✗

8. Program and save the desired information for frames four through fifteen (see Operation, Program Data). A typical format would be the origination call letters in frames 4&5, the destination call letters in frames 6&7, contact telephone number in frames 8-11, latitude in frames 12&13, and longitude in frames 14&15.

9. The SGR38 is shipped with the VITX, VIRX and ENBL functions disabled. See the RS-232C section for more information.

NOTE: The SGR38 is shipped factory aligned and tested.

```
**********************************************
*   Do NOT make any unnecessary adjustments  *
**********************************************
```

Mechanical:

size	19" wide, by 10" deep (including connectors), x 1.75" high (one rack unit).
weight	appx 10 lbs.
rear panel	IEC power connector with EMI/RFI filter
	3AG type fuse holder
	126-218, female five pin, RS-232C
	UG1094/U, female BNC, video input
	UG1094/U, female BNC, program video output
	UG1094/U, female BNC, monitor video output
	UG1094/U, female BNC, exciter control output
front panel	eight character red LED display with mounting bezel
	six pushbuttons for mode selection, operation and data programming

Electrical:

Video Input	1Vpp +/-3dB, 75 ohm termination return loss >36dB DP<.5deg. DG<.5%
Video Output	1Vpp nominal into 75 ohms (75 ohm resistive output)
Exciter Output	TTL level, DO NOT TERMINATE! logic high =>2.4V = exciter ON
Power	115VAC, 60Hz, 8W nominal ********** * ! CONNECT TO GROUNDED OUTLET ONLY ! * **********
RS-232C	+/-10V, 300 baud, no parity, 8 bits, bit 8=0, asynchronous.
VI Data	10 characters per second, frames 16-19, 7 bit ASCII in the range of 20H to 5AH

SGR38 OPERATION:

Front Panel:

```
**********************************************************
* An abbreviated set of operation instructions is silk *
* screened on the left side of the front panel.  It is *
* recommended that the user become familiar with them. *
**********************************************************
```

Detailed Operation:

The front panel contains six pushbutton switches which are externally accessed, and one four position DIP switch which is internally accessed. Together, these switches permit normal operation and programming of the unit.

o Pushbuttons:

MODE selects the mode display stack

DSP selects the particular display stack for a given mode

DEC decrements the selected stack

INC increments the selected stack

ENTER enters new data in the PGM DATA mode and advances to the next character;
  or toggles ON/OFF the control bits in the STATUS mode (provided the ENBL bit is ON)

PGM programs new data in the PGM DATA mode and advances to the next frame number;
  or programs a new control bit in the STATUS mode and advances to the next bit (ENBL must be ON);
  or implements the requested action in response to a " ? " prompt

o DIP switches:

#4 selects the TDM Test Mode, MUST be OPEN in normal operation

#3 inhibits front panel programming when CLOSED

#2 inhibits auto clock set from a net source when CLOSED

#1 selects the CLK ADJ routine when CLOSED on power up, and MUST be OPEN in normal operation

Functional Operation Description:

The front panel allows the user to display and control the various modes of operation. There are eight basic MODEs which are arranged in a stack, as follows;

SID IN	displays the incomming SID information
SID OUT	displays the generated SID information
DATA IN	displays the incomming Data in frames 4-15
DATA OUT	displays the generated Data in frames 4-15
PGM DATA	programs the generated Data in frames 4-15
XFR DATA	transfers the Data from RAM into EEPROM
CLOCK	displays the Real Time Clock information
STATUS	displays the current status information

o Select a Mode:

To select a mode, press the MODE pushbutton; one of the above displays will be shown; this is the current mode. To change the current mode press the INC or DEC pushbuttons until the desired mode is displayed.

o Display a Mode:

Push DSP to display the various information present within the selected mode.

Within each mode is a display stack for that mode. Push INC or DEC to display the desired information.

o Exit a Mode:

To exit a mode push the MODE pushbutton. The display will show the current mode and allow you to select another mode.

o Answer the " ? " Prompt:

If a " ? " prompt is displayed within a display stack, pushing PGM will implement that function, pushing MODE will exit the stack.

o Program Data:

To program data to be inserted into the SID signal on frames 4-15, select the "PGM DATA" mode.
Press DSP, and the display will show "04=ABCDE"
where ABCDE is the current data for frame #04.
One of the characters will be underlined, it is that character which will be changed by pressing DEC or INC.

Holding INC or DEC down for more than one second will cause the character stack to be altered at a 6Hz rate (this will occur only in the PGM DATA mode).

When the desired character is reached, press ENTER. This will advance to the next character. The range of permissable ASCII characters is from 20H to 5AH. This includes punctuation, numbers, and upper case letters. The [ ] brackets are reserved for one of the RS-232C functions.

When all the characters for a frame are selected and as desired, press PGM to advance to the next frame (current frame number plus two). Only frames 4,6,8,10,12,14 can be programmed. Frames 5,7,9,11,13,15 are automatically loaded with the same information.

o Save Programmed Data:

The "PGM DATA" mode should be followed by a "XFR DATA" mode to store the information in non-volatile memory.

To save the programmed data in RAM to EEPROM, select the "XFR DATA" mode. Press DSP. Press PGM in respones to the " XFR ? " prompt to store the data; press MODE to exit. Storage takes about .5 seconds at which time the display will show "DONE". Press MODE to return to the mode stack.

o Set Time:

To set the internal clock, select the CLOCK mode. Press INC or DEC until the display shows " SET ? ". Press PGM to implement setting the time. The display will show "WAIT xy" where xy=the incomming SID seconds. When xy=00 the clock will be set to the incomming SID time, provided that no reception errors occurred. If you attempt to set the clock when incomming SID is absent, the display will show "NO INPUT". Press MODE to exit.

The SGR38 also has an auto clock set function which is activated if incomming SID is present, is a source number between 32 and 47, has its test bit set to a one, and the Auto Clock Set DIP switch (#2) is set to the OPEN position. If the above conditions are met the RTC will be set once each minute to the incomming SID time. The display will show "TIME SET" for one second to indicate that the software clock has also been updated. (This display will also occur when input video is removed.)

TDM Test Mode NOT ACTIVE

This mode simulates reception of the line ten control code. Be sure to disable this mode when in normal operation.

To enter the TDM test Mode:

Set DIP switch #4, to a "0" = CLOSED.

The Display will show:

```
LEFT - 1 2 3 4 5 6 7 8 - RIGHT
       1 0 0 0 0 0 0 x
```

Use front panel switchs to toggle each bit 3 - 7.

Bit designations are as follows:

1: Start Bit, always high

2: Scramble Start Flag, not alterable in this test

3: Scramble, toggle with MODE switch

4: Not Full, toggle with DSP switch

5: TDM Control, toggle with DEC switch

6: A or B, toggle with INC switch

7: In Sync, toggle with ENT switch

8: Frame Count, flashes 1/0 at 30 Hz rate

The exciter control output and APL correction circuits will respond to changes in bits 3 through 7 as required.

****
* DIP switch #4 MUST be OPEN for normal operation *
****

Maintenance:

```
**********************************************************
* The SGR38 is shipped factory aligned.  NO adjustments *
* should be necessary.  The following procedures are to *
* enable qualified personnel to repair and re-establish *
* normal operating conditions to a unit should the need *
* arise!                                                *
**********************************************************
```

Program Video: Video PC, left & middle

1. Apply a 1Vpp test signal with a 100IRE white reference, such as EIA color bars, to the Program Video Input.
2. Connect a waveform monitor to the Program Video Output; H rate trigger.
3. Connect a DC coupled wideband oscilloscope to the Monitor Video Output; H rate trigger, .2V/cm.
4. Terminate both outputs with 75 ohms.
5. Adjust PGM GAIN control for 1Vpp display on the waveform monitor.
6. Verify the oscilloscope DC zero volt reference.
7. Adjust PGM DC control to display blanking at zero volts on the wideband oscilloscope.

Clock Oscillator: main PC, middle.

1. Turn off power to the SGR38.
2. Set DIP switch #1, behind front panel, to CLOSED, pushed towards the PC board.
3. Turn on power. The front panel display should show "CLK ADJ"
4. Connect a frequency countr to the 16.384KHz test point.
5. Adjust CLK ADJ trimmer capacitor for a counter reading of 16.3840KHz. Use of a 10 second gate time is recommended.
6. Push ENTER to exit the CLK ADJ mode. Note: do NOT exit by removing power.
7. Place DIP switch #1 in the OPEN position.
8. Select the CLOCK mode via front panel switches. Display shoud show 11/11 11:11:11 and counting.
9. The Clock should now be set via a terminal or by incomming video with valid SID.

Master Oscillator: main PC, lower left.

1. Connect a frequency counter to the 8.05594MHz test point.
2. Adjust OSC ADJ trimmer capacitor for 8.059943MHz.

   OR

3. Remove any Program Video from the input.
4. Connect the Program Video Output to an externally referenced waveform monitor; H rate trigger, clamp disabled.
5. Terminate the Program Video Output with 75 ohms.
6. Observe black video, no burst, no setup, on the waveform monitor.
7. Adjust OSC ADJ trimmer capacitor for minimum drift on the waveform monitor display.

SID Offset: main PC, lower right.

1. Apply a 1Vpp color bar test signal to the Program Video Input.
2. Connect a waveform monitor to the Program Video Output.
3. Terminate the Program Video Output with 75 ohms.
4. Observe line 20, field 1 of the vertical interval.
5. Adjust TxSID Offset ADJ control for equal SID and video black levels.

APL: main PC, lower right.

1. Apply a 1Vpp 100IRE full field white test signal to the Program Video Input.
2. Connect a waveform monitor to the Program Video Output; H rate trigger.
3. Terminate the Program Video Output with 75 ohms.
4. Place DIP switch #4, behind the front panel, to CLOSED. The front panel display will show a series of 1s & 0s. Use the front panel pushbuttons to obtain a display of "1 0 0 1 1 1 1 x" where x=flashing 1/0. (Reference TDM Test Mode elsewhere in this manual.)
5. Adjust APL ADJ B control for zero volt black level.
6. Apply a full field black (without setup) test signal to the Program Video Input.
7. Adjust APL ADJ W control for 100IRE white level.
7. Return DIP switch #4 to the OPEN position.

RS-232C Port:

The SGR38 permits communications with external computers, terminals, or semi-intelligent modems. The baud rate is fixed at 300, NO Parity, 8 bits with bit 8=0, one stop bit.

The five pin mating connector (Amphenol P/N 126-217) should be wired as follows:

pin A = RXD In, from terminal
B = TXD Out, to terminal
D = DTR Out, to modem
E = CTS In, from modem
H = GND, circuit ground

The command format to the SGR38 is ~~an ESC (1BH) followed by~~ the two digit command, followed by data if required, followed by ~~an ETX (03H).~~ CARRIAGE RETURN (0DH)

The following COMMANDs are recognized by the SGR38:

RM Release Modem - toggles the DTR line to hang up an auto answer modem.

XD Transfer Data from RAM to EEROM, same as XFR DATA mode.

CS MM DD HH MM - Clock Set - sets the internal RTC to the Month Day Hour Minute (and 00 seconds).
ie. CS07041420 will set the clock to July 4, 02:20:00 PM
This command should be sent at a 00 seconds transisition to assure proper shnchronization of the RTC.
The RTC operates in a 24 hour format.

CA Clock Adjust - places the SGR38 in the Clock Adjust mode, which is for test purposes ONLY.
CAUTION: Further communications will be inhibited until the front panel ENTER pushbutton is pressed.

DI xy - Data In Frame # xy - requests the return of the information present on frame xy of the incomming SID signal. The unit will transmit a DIxy= response. xy may be in the range of 04-15.

DO xy - Data Out In Frame # xy - requests the return of the information being generated on frame xy of the outgoing SID signal. The unit will transmit a DOxy= response. xy may be in the range of 04-15.

VALLEY STREAM GROUP, LTD.

28 FOURTH STREET
VALLEY STREAM, NY 11581
516-568-9449

*** PROGRAMMING NOTICE ***

In addition to programming the unit via the front panel switches, the MSGR-38 supports a serial protocol.

The command format to the MSGR-38 is: the two digit command header, followed by data (if required), followed by a carriage return.

i.e. I D M E D I A cr

The following commands have been added to the MSGR-38:

ID a b c d e - Program ID name - loads the data specified by abcde into the syndicator ID field (frames 20,21). The data may be ASCII characters in the range of 20H to 5AH.

TT a b c d e - Program Title - loads the data specified by abcde into the title field (frames 22,23). The data may be ASCII characters in the range of 20H to 5AH.

EP a b c d e - Program Episode - loads the data specified by abcde into the episode field (frames 24,25). The data may be ASCII characters in the range of 20H to 5AH.

Each of the above commands automatically stores the data in non-volatile EEPROM. There is no need to follow them with an XD command.

SI SID IN - requests the return of incomming SID data. The unit will transmit a SI= response.

SO SID OUT - requests the return of generated SID data. The unit will transmit a SO= response.

PD xy ddddd - Program Data In Frame # xy, data 1-5. same as the PGM DATA mode except accessed remotely. xy may be equal to 04,06,08,10,12,14.

ID xxxxx
TT xxxxx
EP xxxxx

LS xyz - Load Source - Loads a new source number for generated SID signal. xyz may range from 000 to 255. This should be followed by an XD command to save the information in EEPROM.

QS Query Status - requests the return of the current status bits. The unit will transmit a Status response.

QT Query Time - requests the return of thr RTC data. The unit will transmit a Time response.

ED ddddddddddd - Encode Data in Frames # 16-19, data 1-10. Data from a terminal or modem may be sent in the VI on frames 16-19 (ten characters per second), provided the status bit VITX=ON. Reception at a remote location must have its status bit VIRX=ON. Some restrictions apply: this command will be followed by the transmission of an XOFF command from the unit, indicating that the buffer is full. After the next frame 19 passes, the unit will send an XON command to allow further data reception. Sending additional data prior to the reception of the XON command will overwrite the previous data. At the receive end, data removed from the VI frames 16-19 will be transmitted bounded by the [ ] markers to deliniate it from responses from commands.

TB 1/0 - Test Bit 1 or 0 - sets the state of the generated SID test bit to a 1 or 0.

BS 1/0 - SID ON/OFF - turns on or off the frame 2-3 portion of the SID signal. ENBL must be ON.

BD 1/0 - Data ON/OFF - turns on or off the frame 4-15 portion of the SID signal. ENBL must be ON.

BT 1/0 - VI Transmit - turns on or off the frame 16-19 portion of the SID signal. ENBL must be ON.

BR 1/0 - VI Receive - turns on or off reception of frame 16-19 SID data. ENBL must be ON.

RESPONSE listing:

DIxy=ddddd: echos the DI header & frame number (xy) followed by the five characters in frame xy. Returns DIxy= : if no data or SID absent.

DOxy=ddddd: echos the DO header & frame number (xy) followed by the five characters in frame xy.

SI=xyzMMDDHHMMSSTb echos the SI header followed by the received SID data xyz=source number, MMDD=month/day, HHMMSS=hour:minute:second, Tb=test bit value. Returns SI=NO SID if SID absent.

SO=xyzMMDDHHMMSSTb echos the SO header followed by the generated SID data. the format is the same as SI=.

Status response= SOxDAxTXxRXxTBxENx where x=0 or 1, SO=Sid Out, DA=Data Out, TX=VITX Enable, RX=VIRX Enable, TB=SID Test bit out, EN=ENaBLe bit.

Time response= MMDDHHMMSS from the real time clock.

Sample Commands & Responses:

NOTE: the STX/ETX must be sent. These control characters can be generated on some terminals by CTRL B & CTRL C, or in basic by the use of the CHR$(n) statement.

Set Time: format= STX C S 0 3 0 8 1 5 4 3 ETX
HEX value= 02 43 53 30 33 30 38 31 35 34 33 03

This will set the clock to March 8, 03:43:00 PM.

Query Time: format= STX Q T ETX
HEX value= 02 51 54 03

The response will be: STX 0 3 0 8 1 5 4 3 1 2 ETX
indicating the date is 03/08 and time is 15:43:12

IN CASE OF DIFFICULTY

Technical assistance is available from 9AM to 5PM Eastern time, Monday through Friday. Please call the number listed below.

Should it become necessary to return a faulty SGR-38 SID Generator Reader for repair, please obtain a Merchandise Return Authorization (MRA) number from Valley Stream Group, Ltd. before shipping the unit.

The MRA number can be obtained from:

Valley Stream Group, Ltd.
[redacted]
Valley Stream, NY 11581

Tel.: (516) [redacted]
568 9449

MARYANN
DeANGELO
(301) 498-4422

VALLEY STREAM GROUP
28 FOURTH STREET
VALLEY STREAM, N.Y. 11581

PARTS LIST

qty	part number	description	reference
1	74HCU04N	hex inverter	L-A1
3	74HC164N	shift register SI/PO	L-A9, F-A1,A2
2	74HC165N	shift register,PI/SO	F-A4,A5
1	74HC221AN	dual one shot	L-A20
1	74HC573N	latch, 8 bit	L-A5
1	74HC4046N	phase locked loop	L-A16
1	74HC4538N	dual one shot	L-A19
1	74LS32N	quad OR gate	L-A21
1	P80C318H	microcontroller	L-A2
1	M81C55	RAM, I/O, timer	L-A4
1	P82C55A	extended I/O	L-A8
	EP310	logic array, SGR3	L-A13
1	EP600	logic array, SGR6B	L-A12
1	EP900	logic array, SGR9	L-A15
1	D27C64	uV-EPROM, 8Kx8	L-A6
1	X2444P	EEPROM, 256 bit	L-A7
1	MM58174AN	real time clock	L-A10
1	PD2816	display, 8 character	F-A3
1	CD4066BE	quad switch	L-A11
1	CD4517BE	daul 64 bit SR	L-A14
1	NE5532AN	dual op amp	L-A24
1	NE5539N	video amplifier	V-A1
1	MC1496P	multiplier	V-A2
1	LM310N	buffer	L-A26
2	LM318N	amplifier	L-A22, A27
1	LM319N	dual comparator	L-A18
2	LM393N	dual comparator	P-A1, A2
	LM741CN	op amp	L-A17
	LM2935T	+5 V regulator	P-VR1
1	MAX232CPE	RS-232 interface	L-A3
1	IH5341CPD	dual RF switch	L-A25
1	MC7808CT	+8 V regulator	P-VR2
1	MC7909CT	-8 V regulator	P-VR3
6	1N4003	diode	P-D1-D6
3	1N5818	diode	P-D7-D9
2	1N5226B	3.3V zener	P-D10, L@A26
1	1N5240B	10V zener	V-D4
4	1N4148	diode	V-D1-D3, L@A26
4	MBR030	diode	L@A11, L@A25
3	2N3904	NPN transistor	L@A17, V-Q3,Q4
3	2N3906	PNP transistor	L@A17, V-Q2,Q5
2	2N4427	NPN driver	V-Q6,Q7
1	2N4265	NPN switch	V-Q1
1	X32768	32.768KHz crystal	L@A10
1	X8.05M	8.055943MHz crystal	L@A1

qty	part number	description	reference
1	76PSB04	4 position DIP switch	
4	TPD11CG-PC-0	pushbutton	
4	IDH-10LP-S3-TG	10 position male header	
4	IDS-10PK-SR-TG	10 position female plug	
1	ICA-406-S-TG	40 pin socket	L-A15
1	ICA-286-S-TG	28 pin socket	L-A6
1	ICA-246-S-TG	24 pin socket	F-A3
1	ICA-243-S-TG	24 pin socket	L-A12
1	ICA-203-S-TG	20 pin socket	L-A13
1	ICA-083-S-TG	8 pin socket	L-A7
1	126-217	5 pin male plug, RS-232	
1	126-218	5 pin female socket, RS-232	
1	A01GEN2D23	line EMI/RFI filter	
1	HKP-CC	fuse holder	
1	F308	.187A fuse	
1	17250	line cord	
1	17536C	right angle line cord	
1	2311	Hubble AC connector	
1	LP-16-350	transformer, +5V	
1	LP-20-300	transformer, +/-8V	
4	UG-1094-U	female BNC	
1	22463R-04	display bezel	
1	BR2/3ABH	battery holder	
1	BR2/3A	lithium battery	
46	C320C104K5R5CA	.1uF @ 50V	
7	199D335X9016A	3.3uF @ 16V T	
32	199D224X9016A	22uF @ 16V T	
3	20YF220	220uF @ 10V E	
2	P6045	1000uF @ 25V E	
1	P6032	2200uF @ 16V E	
1	23PS156	560pF polystyrene	
1	23PS210	1000pF polystyrene	
3	P4551	1000pF mylar	
6	P4525	.1 @ 50V mylar	
1	P4533	.47 @ 50V mylar	
2	DM5-050J	5pF M	
1	DM5-120J	12pF M	
2	DM5-220J	22pF M	
1	DM5-330J	33pF M	
2	DM5-470J	47pF M	
2	DM5-620J	62pF M	
1	DM5-680J	68pF M	
3	DM5-820J	82pF M	
2	DM5-301J	300pF M	
2		9-35pF trimmer	

Resistors:

qty	RN55D-	value 1% MF
1	14R7F	14.7
1	60R4F	60.4
1	75R0F	75.0
6	1000F	100
1	2000F	200
1	3320F	332
2	4420F	442
2	4750F	475
2	6810F	681
2	7500F	750
1	9090F	909
4	1001F	1.00K
1	1211F	1.21K
1	1691F	1.69K
3	2001F	2.00K
1	2321F	2.32K
5	2551F	2.55K
7	3321F	3.32K
2	5111F	5.11K
1	5621F	5.62K
1	9091F	9.09K
11	1002F	10.0K
2	1102F	11.0K
2	2002F	20.0K
1	2322F	23.2K
1	3322F	33.2K
1	3652F	36.5K
1	4322F	43.2K
2	5112F	51.1K
1	8452F	84.5K
2	1003F	100K
1	2553F	255K
1	3323F	332K
1	1004F	1.00M
1	10M	10M
2	CEG53	5K pot
1	CEG14	10K pot
1	CFG22	200 pot
1	CFG53	5K pot
1	Q5104	100K SIP
1	Q7104	100K SIP

Circuit Locations:

The electronics are functionally grouped on four printed circuit boards, Power, Video, Logic and Front.

Power - the power board contains two small transformers, rectifiers, filters, and regulators required to produce +5VDC and +/-8VDC. The primary is passed through a filter, fused, protected by a ZNR and line-to-ground and neutral-to-ground capacitors. The DC regulators have protection diodes on their outputs. The power-on sequencer and power-on-reset are generated on this board.

Video - this board contains the input buffer amplifier, 2X1 switch for inserting SID, and output video driver amplifier. This board mounts on the rear panel over the BNC connectors. Program GAIN and DC level adjustments are on this board.

Logic - this board contains all the controlling and logic functions, the microprocessor, program memory, RS-232C interface, phase locked loop, oscillator, 32 byte non-volatile EEPROM, RAM, real time clock with battery back-up, sync generator and exciter control; as well as the analog portions required to perform clamping, sync and data extraction, SID and black signal generation and APL correction. Adjustments for the 8.05594MHz master oscillator, the 16.384KHz clock oscillator, SID offset level, and APL white & black levels are on this board.

Front - this board contains the LED display and pusbuttons, and additional DIP switches. It is mounted against the front panel.

NOTE: the back-up power for the real time clock is a lithium battery. Care should be taken to avoid shorting the battery terminals.

Circuit Description:

The program video enters via a female BNC, and terminates in 75 ohms. A non-inverting amplifier (NE5539) buffers the signal for distribution to; the PGM-2X1 (MC1496), the APL integrator and the first low pass filter. The output of the first LPF feeds the back porch clamp amplifier (LM318 & GAP-01), the SID/TDM data comparator (LM319), a peak detector, (2N3904 & 2N3906) and an additional LPF for the sync comparator. The output of the peak detector, is divided by 2 to provide a 50% slice of input sync, which yeilds a clean, stable soure of composite sync. The peak detector output is scaled (LM741) and fed to the SID/TDM comparator to provide a 50% slice of data.

Since the received SID Input and the TDM data are the same level (50 IRE), one comparator can be used to extract both data trains.

The PGM composite sync signal feeds a retriggerable one-shot to provide a sync present signal to the uP.

The feedback clamp circuit sets the blanking level of the input video amplifier to zero volts. This permits a clean deletion/insertion of SID and APL information. The timing pulses are derived from two dual one-shots. A 50uSec pulse, which is generated at the trailing edge of sync (HC221), is used to trigger a 2uSec pulse (HC4538), which gates the "A" portion of the the GAP-01 sample & hold. The error voltage is amplified and fed to the negative terminal of the video input buffer amplifier. When input video is absent, the processor disables the clamp pulse and enables the "B" portion of the GAP-01, forcing its ouput to zero.

The APL integrator is buffered and scaled (NE5532A), and fed to one input of the SID/APL-2X1 (IH5341). The second input to this 2X1 is internally generated SID or SID & SYNC depending on the mode of operation. The SID/APL-2X1 output is the second input to the PGM-2X1. Thus, the PGM-2X1 output can be; 1. input video, 2. SID only, 3. SID & SYNC, 4. APL correction. Control of the two 2X1s is such that any combination of switching is available.

Two Programmable Logic Arrays (PLA) EP310 & EP900 control the following functions; 64H PLL, SID output, SID input, TDM input, Exciter output and PGM-2X1.

The 64H PLL (HC4046) is an edge locked oscillator such that the 1.007MHz clock has a known starting point for each horizontal line (see timing diagram). The VCO is set to a nominal 64H or 1.00699MHz, and is divided by 64 in the PLA to produce an H rate square wave. The PLA also provides all the counts from 0 to 63 for producing the required timings for the SID output, the PGM-2X1 control, and the Exciter switch point.

The signal input to the PLL is a non-retriggerable 50uS pulse from the Horizontal Drive one-shot (HC221). This signal is also used to synchronize the PLL counter, and the various line starting points.

The phase locked 64H clock is used to shift the transmit SID information out of its shift register (CD4517). Selection of the proper line is performed by the processor which sets an enable line high prior to the leading edge of sync. Circuits in the PLA generate a gated 1.007MHz clock to the shift register. In addition, the PGM-2X1 will be switched to insert the SID signal into the program video.

The transmit SID output signal from the EP310, is fed to a summing amplifier (LM318), with inputs of SYNCGEN (the internal Sync generator PLA) which is normally off, and an offset which places the amplifier output at zero volts. The summing amplifier output is fed to a shaping network, to approximate a SIN2 shape, and buffered (LM310) before going to the SID/APL-2X1.

The input SID signal is asynchronously clocked into its shift register (CD4517) by circuits in the EP900 PLA. The 8.055MHz clock is divided by eight to provide a 1.007MHz shift clock which is displaced by one-half a bit period. The start bit of the SID signal enables the divide by eight counter, and 48 shifts later disables the counter.

The TDM input data is clocked into an eight bit shift register (HC164) in a manner similar to the input SID. This time the 8MHz clock is divided by 32 to provide the proper clock. The divisor is selected in the PLA in response to the uP control.

The Exciter switch output is formed in the EP900. The switch point is referenced to the 64H phase locked clock. In normal TDM operation, the switch will occurr at the 22nd count of 1.007MHz on line 15. In the asynchronous TDM mode, the switch will occurr at line 12 (OFF) and at line 18 (ON). The Exciter Output (LS32) is a TTL level signal with positive logic; a "ONE" (>2.4V)= exciter ON. The actual on-off sequence of the exciter switch is controll by the TDM signal on line 10. In the absence on any TDM signal, the exciter switch output will be high.

The PGM-2X1 is switched during the active portion of line 20, field 1, to insert the new SID signal. The PLA output is buffered in an OR gate (LS32) and then feeds the 2X1 switch (2N4265). The PGM-2X1 is also continuously enabled upon loss of program video. This forces the Program Video Output to the internally generated SID & SYNC.